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Refine Search

Search Results -

Terms	Documents
L31 and prefetch$	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L32

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, May 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L32	L31 and prefetch$	0	L32
L31	5361337.pn.	1	L31
L30	L28 and (cache$ near9 miss$)	17	L30
L29	L28 and (reduc$ or eliminat$ or minimi$) near4 (cache$ near9 miss$)	0	L29
L28	L27 and switch$	189	L28
L27	(context$ near5 resum$)	234	L27
L26	l1 and (context$ same resum$)	1	L26
L25	l2 and (context$ same resum$)	1	L25
L24	l3 and (context$ same resum$)	0	L24
L23	l4 and (context$ same resum$)	0	L23
L22	l16 and (context$ same resum$)	0	L22
L21	16 and (context$ same resum$)	760	L21
L20	L19 and context	1	L20
L19	L18	1	L19

L18	6237073.pn.	1	L18
L17	6,047,363.pn.	1	L17
L16	L15 and (thread$ or process$)	5	L16
L15	l4 and (context$ near5 switch$)	5	L15
L14	l7 and (context$ near5 switch$)	0	L14
L13	l7 and (memory$ near4 referenc$) and critical$	1	L13
L12	l7 and (critical$ and memory$) and referenc$	1	L12
L11	l7 and (critical$ same memory$) same referenc$	0	L11
L10	l7 and (critical$ near4 memory$) same referenc$	0	L10
L9	L7 and (prefetch$ same compil$)	1	L9
L8	L7 and prefetch$	1	L8
L7	5784711.pn.	1	L7
L6	5,471,602.pn.	1	L6
L5	L4 and (critical$ near8 memory$)	2	L5
L4	L2 and (prefetch$ near8 memory$) near5 (compil$ or execut$)	39	L4
L3	L2 and (prefetch$ near8 memory$)	111	L3
L2	(reduc$ or eliminat$) near4 cache$ near9 miss$	565	L2
L1	THOMPSON, CAROL.IN.	13	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and (sequen$ or index$)	1

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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Search: L29

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, May 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L29	l1 and (sequen$ or index$)	1	L29
L28	l26 and (constant$ same start$ same register$)	1	L28
L27	L26 and count$	0	L27
L26	3571804.pn.	1	L26
L25	L22 and prefetch$	1	L25
L24	L22 and prefetch$ and count$	0	L24
L23	L22 and sequential$ and prefetch$ and count$	0	L23
L22	(constant near4 start$ near9 register$)	89	L22
L21	l11 and (constant$ or start$) near5 register$	0	L21
L20	l1 and (constant$ or start$) near5 register$	0	L20
L19	l1 and prefetch$ near9 (count$ or number$ or times$)	1	L19
L18	l1 and (execut$ or process$) near9 prefetch$	1	L18
L17	L1 and operating system	0	L17
L16	l1 and (location$ or address$)	1	L16

L15	l1 and (prefetch$ near9 (code$ or program$ Or software$ or modul$))	1	L15
L14	(critical$ near4 memory$ near4 referenc$)	24	L14
L13	l11 and critical$	0	L13
L12	L11 and context and switch and resum$	1	L12
L11	5361337.pn.	1	L11
L10	l1 and (stor$ or sav$ or memory$) near9 prefetch$	1	L10
L9	l1 and prefetch$ near9 (memory$ near9 referenc$)	1	L9
L8	l1 and (exchang$ or switch$)	1	L8
L7	l6 and critical$	1	L7
L6	l1 and (process$ or thread$ or execut$)	1	L6
L5	L4 and prefetch$	1	L5
L4	l1 and (memory$ near9 referenc$) and critical$	1	L4
L3	L1 and prefetch$ and memory and compil$ and (execut$ or process$)	1	L3
L2	L1 and prefetch$ and memory and compil$	1	L2
L1	5784711.pn.	1	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	1

Database:
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US Patents Full-Text Database
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Search: L41

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, May 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=TDBD; PLUR=YES; OP=ADJ			
L41	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	1	L41
DB=DWPI; PLUR=YES; OP=ADJ			
L40	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	1	L40
DB=JPAB; PLUR=YES; OP=ADJ			
L39	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L39
DB=EPAB; PLUR=YES; OP=ADJ			
L38	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L38
DB=USOC; PLUR=YES; OP=ADJ			

L37	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L37
DB=PGPB; PLUR=YES; OP=ADJ			
L36	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	21	L36
L35	(reduc$ or eliminat$ or minimi$) nea5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L35
DB=USPT; PLUR=YES; OP=ADJ			
L34	710/262.ccls.	211	L34
L33	711/2,3,113,169.ccls.	1714	L33
L32	717/151,140,141,127,128.ccls.	849	L32
L31	L30 and (constant$ and start$ and register$)	1	L31
L30	3571804.pn.	1	L30
L29	l1 and (sequen$ or index$)	1	L29
L28	l26 and (constant$ same start$ same register$)	1	L28
L27	L26 and count$	0	L27
L26	3571804.pn.	1	L26
L25	L22 and prefetch$	1	L25
L24	L22 and prefetch$ and count$	0	L24
L23	L22 and sequential$ and prefetch$ and count$	0	L23
L22	(constant near4 start$ near9 register$)	89	L22
L21	l11 and (constant$ or start$) near5 register$	0	L21
L20	l1 and (constant$ or start$) near5 register$	0	L20
L19	l1 and prefetch$ near9 (count$ or number$ or times$)	1	L19
L18	l1 and (execut$ or process$) near9 prefetch$	1	L18
L17	L1 and operating system	0	L17
L16	l1 and (location$ or address$)	1	L16
L15	l1 and (prefetch$ near9 (code$ or program$ Or software$ or modul$))	1	L15
L14	(critical$ near4 memory$ near4 referenc$)	24	L14
L13	l11 and critical$	0	L13
L12	L11 and context and switch and resum$	1	L12
L11	5361337.pn.	1	L11
L10	l1 and (stor$ or sav$ or memory$) near9 prefetch$	1	L10
L9	l1 and prefetch$ near9 (memory$ near9 referenc$)	1	L9
L8	l1 and (exchang$ or switch$)	1	L8
L7	l6 and critical$	1	L7
L6	l1 and (process$ or thread$ or execut$)	1	L6
L5	L4 and prefetch$	1	L5
L4	l1 and (memory$ near9 referenc$) and critical$	1	L4
L3	L1 and prefetch$ and memory and compil$ and (execut$ or process$)	1	L3
L2	L1 and prefetch$ and memory and compil$	1	L2
L1	5784711.pn.	1	L1

Terms used
prefetch and **memory** **reference** and **reduce** and **miss** and **cache** and **context** and **switch**

Found **57,023** of **132,857**

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Display results expanded form

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Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

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Relevance scale ☐■■■■■

1 Comparative evaluation of latency reducing and tolerating techniques

Anoop Gupta, John Hennessy, Kourosh Gharachorloo, Todd Mowry, Wolf-Dietrich Weber

April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture**, Volume 19 Issue 3

Full text available: pdf(1.36 MB) Additional Information: full citation, references, citings, index terms

2 Reducing memory latency via non-blocking and prefetching caches

Tien-Fu Chen, Jean-Loup Baer

September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9

Full text available: pdf(1.36 MB) Additional Information: full citation, references, citings, index terms

3 Hardware-software trade-offs in a direct Rambus implementation of the RAMpage memory hierarchy

Philip Machanick, Pierre Salverda, Lance Pompe

October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 32 , 33 Issue 5 , 11

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms

The RAMpage memory hierarchy is an alternative to the traditional division between cache and main memory: main memory is moved up a level and DRAM is used as a paging device. The idea behind RAMpage is to reduce hardware complexity, if at the cost of software complexity, with a view to allowing more flexible memory system design. This paper investigates some issues in choosing between RAMpage and a conventionalcache architecture, with a view to illustrating trade-offs which can be made in choosi ...

4 Instruction prefetching of systems codes with layout optimized for reduced cache misses

Chun Xia, Josep Torrellas

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd**

Refine Search

Search Results -

Terms	Documents
(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	1

Database:

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DB=TDBD; PLUR=YES; OP=ADJ			
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DB=DWPI; PLUR=YES; OP=ADJ			
L40	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	1	L40
DB=JPAB; PLUR=YES; OP=ADJ			
L39	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L39
DB=EPAB; PLUR=YES; OP=ADJ			
L38	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L38
DB=USOC; PLUR=YES; OP=ADJ			

L37	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L37
DB=PGPB; PLUR=YES; OP=ADJ			
L36	(reduc$ or eliminat$ or minimi$) near5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	21	L36
L35	(reduc$ or eliminat$ or minimi$) nea5 (cache$ near9 miss$) and prefetch$ and (memory$ near9 referenc$)	0	L35
DB=USPT; PLUR=YES; OP=ADJ			
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L33	711/2,3,113,169.ccls.	1714	L33
L32	717/151,140,141,127,128.ccls.	849	L32
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L29	l1 and (sequen$ or index$)	1	L29
L28	l26 and (constant$ same start$ same register$)	1	L28
L27	L26 and count$	0	L27
L26	3571804.pn.	1	L26
L25	L22 and prefetch$	1	L25
L24	L22 and prefetch$ and count$	0	L24
L23	L22 and sequential$ and prefetch$ and count$	0	L23
L22	(constant near4 start$ near9 register$)	89	L22
L21	l11 and (constant$ or start$) near5 register$	0	L21
L20	l1 and (constant$ or start$) near5 register$	0	L20
L19	l1 and prefetch$ near9 (count$ or number$ or times$)	1	L19
L18	l1 and (execut$ or process$) near9 prefetch$	1	L18
L17	L1 and operating system	0	L17
L16	l1 and (location$ or address$)	1	L16
L15	l1 and (prefetch$ near9 (code$ or program$ Or software$ or modul$))	1	L15
L14	(critical$ near4 memory$ near4 referenc$)	24	L14
L13	l11 and critical$	0	L13
L12	L11 and context and switch and resum$	1	L12
L11	5361337.pn.	1	L11
L10	l1 and (stor$ or sav$ or memory$) near9 prefetch$	1	L10
L9	l1 and prefetch$ near9 (memory$ near9 referenc$)	1	L9
L8	l1 and (exchang$ or switch$)	1	L8
L7	l6 and critical$	1	L7
L6	l1 and (process$ or thread$ or execut$)	1	L6
L5	L4 and prefetch$	1	L5
L4	l1 and (memory$ near9 referenc$) and critical$	1	L4
L3	L1 and prefetch$ and memory and compil$ and (execut$ or process$)	1	L3
L2	L1 and prefetch$ and memory and compil$	1	L2
L1	5784711.pn.	1	L1